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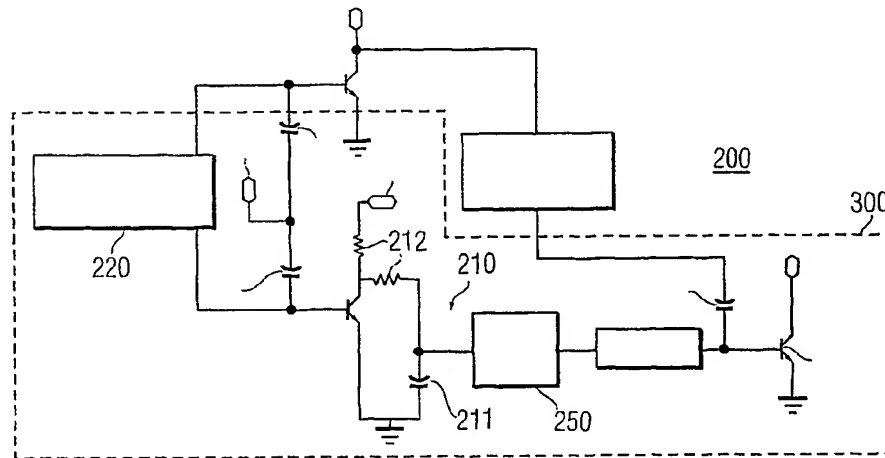
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(54) Title: **SLIDING BIAS CIRCUIT FOR ENABLING DYNAMIC CONTROL OF QUIESCENT CURRENT IN A LINEAR POWER AMPLIFIER**



(57) Abstract: A sliding bias circuit for dynamically controlling quiescent current flowing through an output transistor of a linear power amplifier operating in an output frequency band, the linear power amplifier comprising a circuit device for generating a bias signal producing a quiescent current flowing through the output transistor of the RF power amplifier, the sliding bias circuit comprising a detector circuit for detecting RF input to the amplifier and generating an output signal tracking the detected RF input, the output signal directly coupled to the circuit device for automatically modifying the bias signal and the quiescent current through the output transistor. In this manner, the quiescent current at the output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels.

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SLIDING BIAS CIRCUIT FOR ENABLING DYNAMIC CONTROL OF QUIESCENT CURRENT IN A LINEAR POWER AMPLIFIER

The present invention relates to commonly-owned, co-pending United States Provisional Patent Application Serial No. 60/433,742 [703066, Atty. Docket US020584], the subject matter of which is wholly incorporated by reference herein.

The present invention relates generally to radio frequency (RF) power amplifiers, and, more specifically to a sliding bias circuit for a linear radio frequency (RF) power amplifier for communication devices.

Traditional biasing techniques for Power non-switching Amplifiers (P.A.) comes from the use of a static quiescent current point I_{cq} that provide amplification of current on the whole sine wave (Class A), a partial sine wave (AB), only half (B) or even less (C). The linearity performance of those amplifiers is inversely related to the obtained efficiency as well as the quiescent point. Class AB bias circuits have been used ever increasingly in the past 10 years as they provide a compromise between linearity and efficiency as compared to other Class A, B power amplifiers which exhibit less efficient and/or non-linear characteristics. They involve biasing the P.A. at a relatively low I_{cq} point but not zero to maintain linearity (quiescent current at the collector of the transistor device) and current increases as power level increases. To work properly, the bias circuit needs to present a very low impedance at base band. This is to avoid the amplifier's AM or PM characteristics to be pulled by the bias circuit, creating linearity deterioration.

By nature of the CDMA and WCDMA systems, CDMA Power Amplifiers operate over a broad dynamic range with a relatively good linearity to meet spectrum requirements, but also to retain the quality of the data stream.

Figure 1 illustrates a graph 12 of the power used versus the power delivered, i.e., curve represents probability of occurrence of power level when operating in the field, with most power in use concentrated about the 3 dBm point 15 for example, but not at maximum power level or lowest power level. Additionally superimposed on the graph 12 are curves 20 showing the current dissipated by the power amplifier at the power level that's specified. Several schemes are shown in Figure 1 whereby, a first scheme shows a curve 22 representing a fixed bias of 2.8 volts and a constant quiescent current. As the quiescent level is determined by the performance at the highest power level, power dissipated for bias scheme represented by curve 22 is worst case for all power output levels.

In another curve 24, the bias is manually modified, e.g., at 15 dBm, and in another curve 26, the current is also changed at 5 dBm output power. In a better curve 28, the bias is adjusted dynamically and referred to as a "sliding bias" curve. The best curve 30 shown implements a dc-to-dc converter circuit in the phone to reduce collector voltage in the output transistor device and thus, shows the lowest current use at the higher power levels. It is apparent that as the power increases, the current dissipated is increasing with increased power levels.

Figure 2 illustrates a graph 35 depicting the dissipation of power (integrating over all power levels with the current) for each of the curves shown in Figure 1.

Thus, in view of Figure 1, there is recognized the importance of reducing the current at all power levels, e.g., that are not at maximum power levels, most of the time. The ever-increased importance of the current consumption in the Power Amplifiers requires ever-increased efficiency at all power levels. The importance of current consumption has lead Power Amplifier (P.A.) designers to primarily use Class AB biasing techniques.

When the CDMA P.A. is operating primarily at relatively low power levels (compared to the maximum power required (about 20 to 30dB less)), the current consumption equals the quiescent current. With 2.5G systems, the advent of data transmission in phones as opposed to voice transmission makes the puncturing of the PA's during data stream much more infrequent (puncturing is allowed by voice compression).

Those factors being considered, to increase phone talk time, there is an added emphasis on reducing the I_{cq} (quiescent current) of the Power Amplifier of the future.

The Power Amplifier (P.A.) of the future is a Class AB that needs to provide linearity with an I_{cq} near or equal to zero to provide maximized efficiency at all power levels on a 60dB dynamic range. However, the operation of the Power amplifier at the highest power level is one primary I_{cq} requirement.

To meet both requirements, several schemes to date have been employed, including, as shown in Figures 1 and 2: use of a DC/DC converter, or use of two operating modes to accommodate for high and low power. Various methods can be used to accommodate low and high power levels: switching between two bias current levels, switching between RF line-ups, gain stage bypassing, load switch; the most often being used alternative bias levels.

This sliding bias technique mentioned hereinabove implements a bias circuit that has a near zero impedance or even slightly negative impedance versus power to provide added currents at high power levels. However, this technique has been extremely difficult to implement.

Of all methods, the use of a DC/DC converter yields the best performance, however at a high cost and complexity. To date the usual mean of managing the dissipation issue has been switching between two quiescent currents. However this is becoming insufficient for tomorrow's more competitive requirements.

It would thus be highly desirable to provide a "sliding bias" circuit for a linear power amplifier used in wireless applications that provides optimum efficiency and linearity within the whole dynamic range.

It is an object of the present invention to provide a novel circuit optimized for use reducing amount of quiescent current consumed in a Power Amplifier output stage.

It is another object of the present invention to provide a power amplifier for use in wireless phone and like communications systems employing but not limited to, Code Division Multiple Access (CDMA), WCDMA, and other modulation schemes implementing a novel circuit for optimizing the quiescent current utilized at all power levels.

It is a further object of the present invention to provide a novel bias circuit optimized for use in reducing amount of quiescent current consumed in a Power Amplifier output stage implemented in an integrated circuit.

It is another object of the invention to provide a novel bias circuit optimized for use in reducing amount of quiescent current consumed in a Power Amplifier output stage implemented in an integrated circuit that implements InGaP HBT or other Bipolar transistors including but not limited to: Si-BJT, GaAs-HBT, InP-HBT, SiGe-HBT circuit devices or similar device technology.

It is yet a further object of the present invention to provide a linear power amplifier including circuitry optimized for minimum dissipation and optimal linearity.

In accordance with the principles of the invention, there is provided a sliding bias circuit for dynamically controlling quiescent current flowing through an output transistor of a linear power amplifier operating in an output frequency band, the linear power amplifier comprising a circuit means for generating a bias signal producing a quiescent

current flowing through the output transistor of the RF power amplifier, the sliding bias circuit comprising a detector circuit means for detecting RF input to the amplifier and generating an output signal tracking the detected RF input, the output signal directly coupled to the circuit means for automatically modifying the bias signal and the quiescent current through said output transistor, whereby the quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels.

In a preferred embodiment, the bias circuit means is provided in a radio frequency (RF) linear power amplifier implemented for wireless communication devices includes a sliding bias circuit that produces quiescent current for an output stage amplifier that automatically tracks an RF signal being input to the amplifier at power ranges above a certain power output threshold.

Advantageously, the present invention includes a circuit for reducing amount of quiescent current consumed in a Power Amplifier operating in Class AB. It is preferably implemented in wireless phone and like communications devices operating in accordance with, but not limited to, CDMA, WCDMA or other modulated systems.

These and other features, aspects, and advantages of the apparatus and methods of the present invention will become better understood with regard to the following description, appended claims, and accompanying drawings where:

Figure 1 illustrates a graph 12 of the power used versus the power delivered, i.e., curve represents probability of occurrence of all operating power levels.

Figure 2 illustrates a graph depicting the dissipation of power (integrating over all power levels with the current) for each of the curves shown in Figure 1.

Figure 3 illustrates a two-stage class AB type power amplifier. Figure 4 illustrates a detailed example of a class AB type power amplifier 100 including output stage 110 with its Class AB bias circuit.

Figure 5 illustrates a plot indicating the optimal behavior of a varying I_{cq} vs. output power level (P_{out}).

Figure 6 illustrates a plot 150 of the I_{cq-2} current values versus the input power of the P.A. (P_{in}) over three operating temperature conditions.

Figure 7(a) illustrates an I_{cq-2} current response curve such as curve 180.

Figure 7(b) illustrates a plot 190 of the I_{cq-1} and I_{cq-2} control curves versus the output power (P_{out}) of the P.A. with I_{cq-1} being constant over the operating range and I_{cq-2} that increases at two regions.

Figure 8 illustrates a simplified circuit diagram 200 of the P.A. implementing the sliding bias circuit of the invention.

Figure 9 illustrates the simplified voltage response of the detect circuit 210.

Figure 10 illustrates a detailed circuit diagram 310 according to a preferred embodiment of the invention.

Figure 3 illustrates a class AB type power amplifier 50 implementing as N-type bias circuit. Such a circuit is disclosed in commonly-owned, co-pending United States Patent Application Serial Number 10/189,233 entitled IMPROVED LINEAR POWER AMPLIFIER, the whole contents and disclosure of which are incorporated by reference as if fully set forth herein. Basically, this class AB type power amplifier 50 is shown as a two stage having output gain transistors Q1, Q2 each with a respective coupling capacitor CQ1 and C Q2 for coupling the RF signal and each with its own bias circuit Bias Q1 and Bias Q2, respectively, which dynamically or automatically functions to keep the operating quiescent current (I_{cq}) constant depending upon changing operating conditions and power operations. The RF input is shown coupled to the Q1 gain transistor via the C Q1. The first stage Q1 is matched to the second stage via an interstage impedance matching circuit 55 to optimize the two stage configuration. Figure 4 illustrates an example class AB type power amplifier 100 which may comprise either one of the stages shown in the exemplary circuit of Figure 3 and, is described in commonly-owned, co-pending United States Patent Application Serial Number 10/189,233. For example, there is depicted an RF input 105, an output transistor 110 (e.g., Q1 or Q2) and a static bias current circuit 150 such that the bias current is going to be constant regardless of operating of temperature, variation of RF signal input, etc. The bias circuit 150 basically comprises a current mirror circuit including a transistor 120 that maintains a collector current that mirrors the collector current of the RF output transistor device. In effect, the quiescent current is determined by the current through the transistor 120. On a multistage amplifier this circuit can be used on any stage. The advantage is a temperature stable bias current. The control loop allows the current to be monitored closely and I_{cq} can be minimized as much as possible. Further provided is a Vmode transistor 125 which is a transistor having a voltage ("V-mode") input 126 which

operates under system control (not shown) to discretely modify the quiescent current between two different levels depending upon the V-mode voltage applied. This produces a power dissipation curve such as curve 24 shown in Figures 1 and 2.

For an example P.A. such as shown in Figure 4, a plot indicating the optimal behavior of a varying I_{cq} vs. output power level (P_{out}) was determined and results set forth in Figure 5. In the determination, InGaP and AlGaAs devices have been evaluated at all temperatures, however it is understood that the power amplifier output transistor may comprise HBT or other Bipolar transistors including but not limited to: Si-BJT, GaAs-HBT, InP-HBT, SiGe-HBT circuit devices or similar device technologies. Specifically, it was determined what I_{cq} would be necessary for first and second stages of the P.A. to meet a -46dBc with only a small 1-2dB margin at all power levels, and, additionally, to achieve a minimum gain requirement of 25dB at 28dBm, and of 10dB at all power levels was included. As shown in Figure 5, which is a diagram 140 plotting raw data of $I_{cq1,2}$ v. P_{out} (power out) at room temperature for two stage P.A., it was determined that only the second stage bias I_{cq2} needs to vary with power levels. That is, in a two stage P.A. implementing PCS InGaP devices as shown in Figure 5, it was determined that from about 15dBm it is possible to meet the requirement with a lower I_{cq2} than at lower power levels, as it is very difficult to meet such a requirement as the curve 130 is not monotonous.

As the graph of Figure 5 depicts, the minimum I_{cq} 130a is constant below about 0dBm at 11mA or so. There is a second I_{cq2} plateau 130b at 26 mA or so from 7dBm to 19dBm, before the required I_{cq2} increases significantly. Rather than implement the I_{cq} changes using Vmode control only, a sliding bias circuit is provided that automatically generates such an I_{cq2} curve to accommodate the plateau 130b and the rising curve for the I_{cq2} up to the highest power level. However, it is preferred to use a sliding bias for I_{cq2} at the higher output power levels coupled with Vmode control at the lower power level to accommodate for plateau 130a, as long as it will not interfere with the sliding bias operation. Table 1 indicates an example product specification including I_{cq} values and changes using Vmode control in a sliding bias circuit.

Vmode	Power levels	I_{cq-1}	I_{cq-2}	Total I_{cq} (Ibias not included)
3V	<5dBm	12mA	11mA	~25mA
0V	>5dBm	12mA	26mA	~40mA

Table 1 – Vmode combined with sliding bias

Vmode	Power levels	Icq-1	Icq-2	Total Icq (Ibias not included)
3V	<15dBm	12mA	26mA	~40mA
0V	>15dBm	12mA	90mA	~100mA

Table 2 – Vmode, no sliding bias

In Table 1, the values of Icq-1 and Icq-2 represent target values achievable by a sliding bias circuit with Vmode control. For example, the value of 26mA is an approximate minimum for a 28dBm InGaP CDMA P.A. using efficiency enhancement by bias control. Specifically, the Vmode Table 1 explains that by adding a Vmode switch to the sliding bias circuit, there is provided a very efficient mode of operation. The sliding bias circuit takes care of the increase of current at the highest power level. However, the curve shows that the current can again be reduced at powers below 5dm approximately. So the combination is preferred for more efficient operation. It is remarkable to compare Table 2 provides the quiescent current values that would result when implementing Vmode system bias control without the sliding bias circuit implemented. As compared to the values in Table 1, the quiescent currents are significantly higher.

It is understood that it is within the purview of skilled artisans to possibly achieve lower values of Icq-2, e.g., using a line-up switching method rather than quiescent current switching.

In addition to the use of Vmode Icq-1 and Icq-2 control, the use of a sliding bias circuit requires detection of the input power at the device to control. This requirement comes directly from the variation of the required current with the power level, measured at the input or at the output). As the quiescent current of the 1st stage is not required to change, the power can be advantageously detected at the input using a current detector biased jointly with Q1. As the quiescent current of Q1 is tightly controlled, so will the detector be as well.

Figure 6 illustrates a plot 150 of the Icq-2 current values versus the input power of the P.A. (Pin) over three operating temperature conditions, i.e., hot 160, room temperature 165 and cold 170. Figure 7(a) particularly illustrates a plot 175 summarizing the Icq-2 current values 180 as function of the input power (Pin) of the P.A. acceptable over all

temperatures (hot, room, cold). The sliding bias circuit of the invention is thus configured to achieve an I_{cq-2} current response curve such as curve 180 shown in Figure 7(a). Figure 7(b) illustrates a plot 190 of the I_{cq-1} and I_{cq-2} control curves versus the output power (P_{out}) of the P.A. with I_{cq-1} being constant over the operating range and I_{cq-2} shown increasing at two regions. One region which is increasing after 20 dBm is to be handled by the sliding bias circuit and increasing at 5 dBm via Vmode control as in Table 1.

Figure 8 illustrates a simplified circuit diagram 200 of the P.A. implementing the sliding bias circuit of the invention. As shown in Figure 8, the P.A. 200 is a class AB type power amplifier as in Figure 3 depicted as a two stage having gain transistors Q1, Q2 each with a respective coupling capacitor CQ1 and C Q2 for coupling the RF signal, an interstage match, and bias circuits for Q1 and Q2. Additionally included is a sliding bias circuit 250 for modifying the bias of Q2, and as shown in Figure 8, is illustrated as a separate circuit. It is understood that the Q2 bias and slide circuit may be integrated. As shown in Figure 8, however, the P.A. 200 additionally includes an RF detect circuit 210 for detecting the incident power on the input of the amplifier. The RF detect circuit 210 particularly mirrors the current through Q1 (R_{Fin}) and utilizes the same bias circuit as Q1, represented as a common bias circuit 220. The RF detect circuit 210 comprises a transistor Qd biased at the constant current for class AB operation which, as shown in Figure 8, is used to drive the sliding bias circuit 250. Thus, when power is input to the transistor, the current through the collector increases. The detected current is modified into a voltage through the resistor 212 at the collector of the detector. The value of this resistor 212 is also a factor in the amplitude of the detection. If no reference voltage is available by the phone, a circuit generating the reference should be provided such as a band gap type circuit. The modified voltage signal at the capacitor 211 increases with increasing RF signal input to the detect circuit 210, i.e., voltage tracks the input RF power level. The resistor 212 and capacitor 211 combination at the output of the detect circuit 210 additionally functions as a filter to remove any RF modulation of the tracked voltage signal so that a modulation signal is not fed into the sliding bias circuit 250.

The value of the averaging capacitor 211 is critical to the behavior of the circuit. Too high a value would make the circuit too slow and therefore not pass the system specification for settling the performance of the P.A.; too low and the detector averaging would not be proper. The lack of averaging may create base band modulation at the input

of the sliding bias circuit 250 for Q2. It would then generate some additional Adjacent Channel Power Ratio (ACPR) and the power amplifier would not meet this critical specification.

The detected voltage is used to feed a slide circuit that modifies the quiescent current of Q2 provided by its own bias circuit. There is no modification to the interstage circuit nor the load circuit of Q2.

Figure 9 illustrates the simplified voltage response of the detect circuit 210. The detector transistor Qd is a transistor mirror of Q1 biased with the same current density. The mirror ratio is $r = A_{Qd}/A_{Q1}$ where "A" is the emitter area of the transistor. As shown in the plot of Figure 9, the maximum voltage VdO is for no power through the detector or, a power under the value PdO at which the base of Qd starts to conduct more current. $V_{dO} = V_{ref} - R_0 \cdot I_{cqd}$. Additionally, $I_{cqd} = r \cdot I_{cq1}$. In general, the value of "AQd", or "r" should be chosen as small as possible to maximize the detector range (maximize "VdO").

As the bias is common with Q1, the current quiescent through the RF detector 210 is very stable with temperature and other variables such as other voltage presented to the P.A.. The detector is a mirror of Q1 and as a starting point the value of Cd is proportional to Cq1 with the same mirror ratio. However the input power through the detector 210 may be adjusted by varying the value of detector capacitor Cd so that the detected current starts to slide at the desired level "PdO". In the detector the values of the two resistors 212a, 212b in parallel defines the RF load RLd of the Qd. Again for maximizing the dynamic range of the detector the values of the resistance should be chosen so that $RLd = (V_{ref} - V_{sat})^2 / (2 \cdot PdM)$ where "PdM" is the value of the highest power considered at the output of the detector. As a starting point the value of R212a should be chosen so that at the maximum power level $V_{dM} = V_{ref} - R_{212a} \cdot I_{dM}$ (with resistor 212a the resistor connected to Vref); however it can be reduced if the objective is not to maximize detector range or to fit the detected voltage and the slope of the curve to fit the Bias circuit of Q2 and fulfill the quiescent current requirements defined in Fig 7(a).

The input power detected through tapping at the first stage of the P.A. (current detection) is necessary because of the variation of the current required with the power level. The circuit needs to perform at a "slow" speed and kick in when more power is provided at the input of the P.A. (i.e., not at base-band speed). This consideration is very important because any variation Ic_q at base band would, in turn, change the gain and phase

of the stage in consideration, therefore modulate this stage and generate additional energy in the adjacent channels. The ACPR may then be deteriorated significantly. There is a range of detector capacitors 211 that is allowed by the circuit that allows the detector 210 to average the base band signal but be still fast enough to meet the overall system specification. This range may differ on different systems as the base band frequency varies between systems and the time required for a new power level to settle is also different between systems.

At the input of the slide circuit 250, the voltage tracks the input power level. As Qd is a transistor operating in a Class AB configuration, below a certain power level, there will be no detected voltage and after a certain voltage threshold level, the slide circuit 250 will kick in. There may be some shaping of the signal required in the slide circuit 250, e.g., a resistor, to correct the voltage fed to the Q2 bias if necessary. It is preferred that the sliding bias circuit 250 is integrated with the Q2 bias circuit.

Figure 10 illustrates a circuit diagram 310 according to a preferred embodiment of the invention that represents a portion of the output Class AB P.A. corresponding to the circuit portion 300 indicated in Figure 8. In this embodiment, what is important is the presence of a transistor on the each opposite side of the differential pair 325 so that the circuit keeps operating very well at all temperatures. The sliding bias circuit is connected on the other side of the differential pair 325. It modifies the reference voltage at this port and therefore directly adjusts the quiescent current when power is applied to the detector. The other transistor is biased commonly with Q1 and the RF detector. It is an exact replica of the detector transistor. Only, no RF power is pushed through.

Particularly, as shown in Figure 10, the reference voltage on the other side of differential pair 325 is being modified by virtue of the connection of the RF detector 210' to the input of the differential pair via resistor 326. Thus, the reference voltage at the input to the differential pair will change with the power level detected by the RF detector 210'. Because the voltage reference is altered at the differential pair 325, the control loop is adjusting the current flowing through which mirrors the current at the output of Q2. The bias circuit transistor 225' is included at the opposite input of the differential pair, and is at the same point as the bias point for the detector transistor however, with no RF signal being pushed through. That is, as shown in Figure 10, with no RF applied, the voltage bias 221 at the input to transistor Qd in the RF detector portion 210' is the same as the bias point

221 at the transistor 225' at the other side of the differential pair. This remains true for every condition of temperature etc, maintaining the balance of the circuit.

Thus, in the sliding bias circuit, detected voltage is connected directly to the differential pair. This makes for an easy tuning of the modification of the quiescent current with the power level. By adjusting the resistors of the circuit to get the proper curve as in Figure 9.

It should be understood that, in addition to the sliding bias control, the Vmode transistor 125 shown in Figure 3 for discretely changing the quiescent current via a Vmode signal 126 may be additionally provided in parallel to the sliding bias circuit 225' to provide the additional Vmode discrete quiescent current I_{cq-2} control.

An example output quiescent current flow in a power amplifier stage adjusted dynamically by implementing a sliding bias curve circuit results in a better curve 28, which is shown compared to other methods such as shown in Figure 1. As shown in Figure 2, a sliding bias-type curve 28 is a good method for reducing power dissipated by the communications device (phone). As shown in Figure 1, it is operating close to Class B at low power levels, where linearity, P1 dB, and gain are no issue. The sliding circuit that produces quiescent current for an output stage amplifier that automatically tracks an RF signal being input to the amplifier at power ranges above a certain power output threshold. Thus, it the circuit adjusts the bias point dynamically as the mean RF power incident to the device changes.

While there has been shown and described what is considered to be preferred embodiments of the invention, it will, of course, be understood that various modifications and changes in form or detail could readily be made without departing from the spirit of the invention. It is therefore intended that the invention be not limited to the exact forms described and illustrated, but should be constructed to cover all modifications that may fall within the scope of the appended claims.

CLAIMS:

1. A radio frequency (RF) linear power amplifier (200) operating in an output frequency band, having an output transistor (Q2), said power amplifier comprising:

(a) a circuit means (310, 230', 325, 120) for generating a bias signal producing a quiescent current flowing through said output transistor of said RF power amplifier; and,

(b) a detector circuit means (210') for detecting RF input (RFIN) to said amplifier and generating an output signal tracking said detected RF input, said output signal directly coupled (326) to said circuit means (325) for automatically modifying said bias signal and said quiescent current through said output transistor, whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels.

2. The linear power amplifier as claimed in Claim 1, wherein said circuit means (230', 310, 325) for generating a bias signal producing a quiescent current comprises a differential transistor pair (325a, 325b), said detector circuit means output signal being coupled directly to one side of said differential pair.

3. The linear power amplifier as claimed in Claim 2, further including a sliding bias circuit (250) connected to another side of said differential pair for automatically modifying said quiescent current for an output stage amplifier according to said detected RF signal input.

4. The linear power amplifier as claimed in Claim 3, wherein the sliding bias circuit means includes means (221, 225') for automatically reducing the quiescent current for an output stage amplifier at power ranges below a certain power output threshold.

5. The linear power amplifier as claimed in Claim 1, comprising first and second power output stages, wherein said detector circuit means detects RF input to said amplifier at said first output stage (Q1), for reducing said quiescent current at a second output stage (Q2).

6. The linear power amplifier as claimed in Claim 1, further comprising means (125, 126) for further modifying said quiescent current at a second output stage under

discrete voltage control.

7. A device including a radio frequency (RF) linear power amplifier (200) operating in an output frequency band, having an output transistor (Q2), said power amplifier comprising:

(a) a circuit means (310, 230', 325, 120) for generating a bias signal producing a quiescent current flowing through said output transistor (Q2) of said RF power amplifier;

(b) a detector circuit means (210') for detecting RF input to said amplifier and generating an output signal tracking said detected RF input, said output signal directly coupled (326) to said circuit means for automatically modifying said bias signal and said quiescent current through said output transistor, whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels.

8. The device as claimed in Claim 7, wherein said circuit means (310, 325) for generating a bias signal producing a quiescent current comprises a differential transistor pair (325a, 325b), said detector circuit means output signal being coupled directly to one side of said differential pair.

9. The device as claimed in Claim 7, further including a sliding bias circuit means (221, 225') connected to another side of said differential pair for automatically modifying said quiescent current for an output stage amplifier according to said detected RF signal input.

10. The device as claimed in Claim 7, further comprising means (125, 126) for further modifying said quiescent current at a second output stage under discrete voltage control.

11. A sliding bias circuit (250) for dynamically controlling quiescent current flowing through an output transistor (Q2) of a linear power amplifier (200) operating in an output frequency band, said linear power amplifier comprising a circuit means (230', 325, 221, 225', 120) for generating a bias signal producing a quiescent current flowing through said output transistor of said RF power amplifier, said sliding bias circuit comprising:

a detector circuit means (210') for detecting RF input to said amplifier and generating an output signal tracking said detected RF input, said output signal directly coupled (326) to said circuit means (325, 221, 225') for automatically modifying said bias signal and said quiescent current through said output transistor (Q2), whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels.

12. The sliding bias circuit as claimed in Claim 11, wherein said circuit means for generating a bias signal producing a quiescent current comprises a differential transistor pair (325a, 325b), said detector circuit means output signal being coupled directly to one side of said differential pair.

13. The sliding bias circuit as claimed in Claim 11, wherein said linear power amplifier (200) comprises first (Q1) and second (Q2) power output stages, wherein said detector circuit means detects RF input to said amplifier at said first output stage, for reducing said quiescent current at a second output stage.

14. The sliding bias circuit as claimed in Claim 13, wherein said second power output stage further includes means (125, 126) for further modifying said quiescent current at a second output stage under discrete voltage control.

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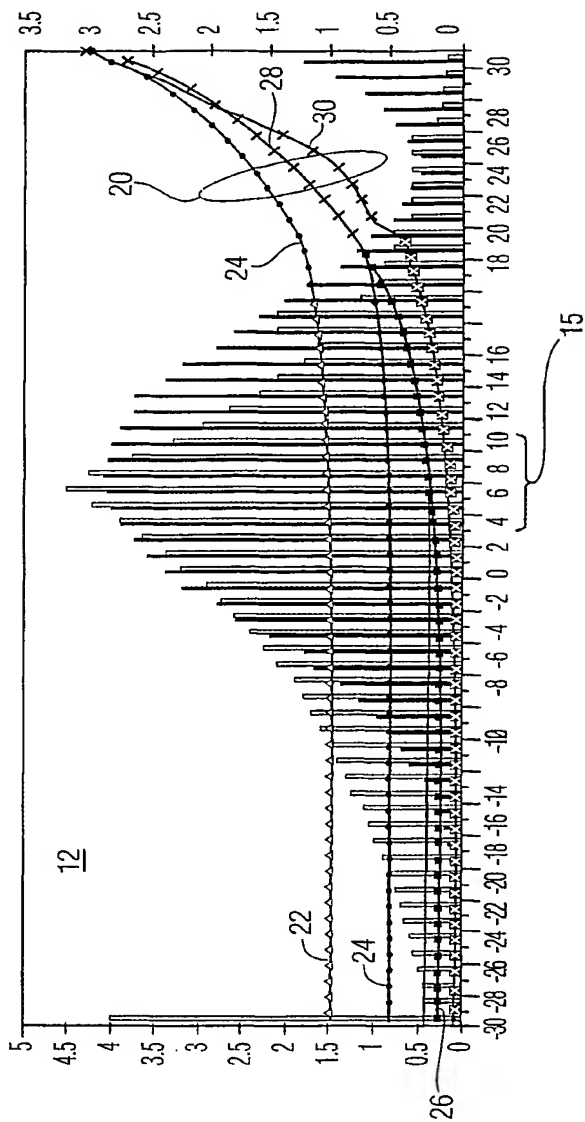
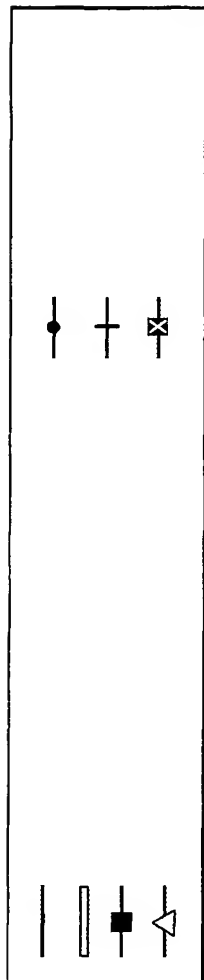


FIG. 1

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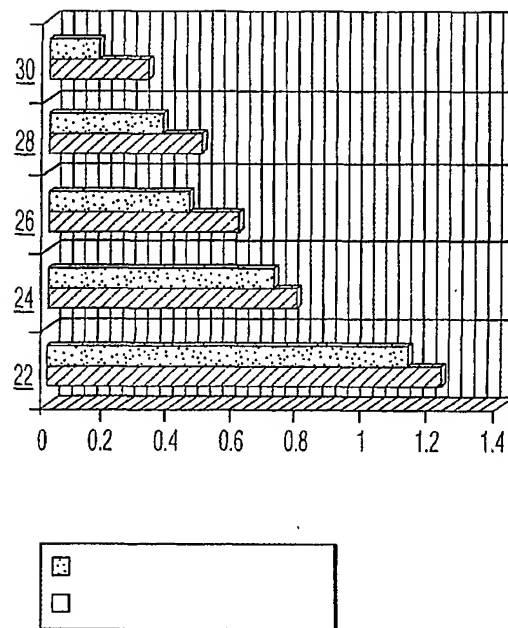


FIG. 2

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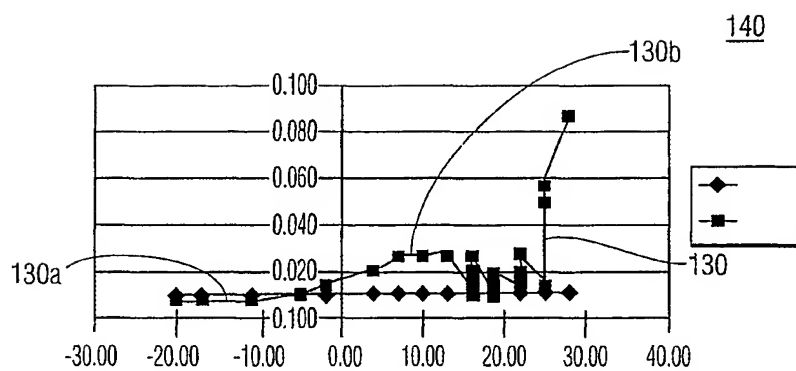


FIG. 5

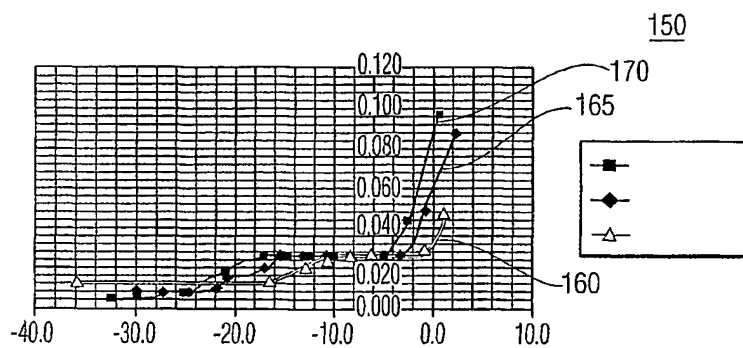


FIG. 6

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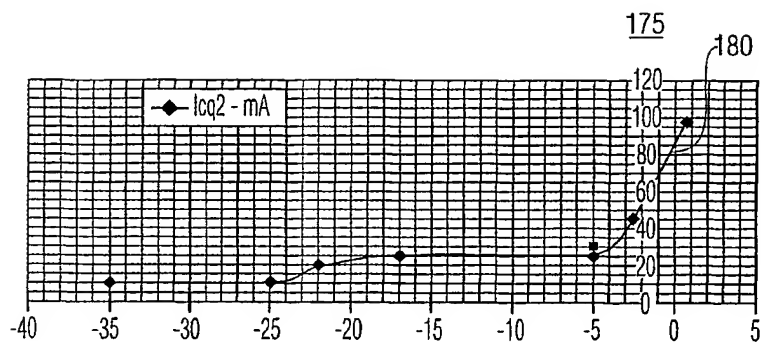


FIG. 7A

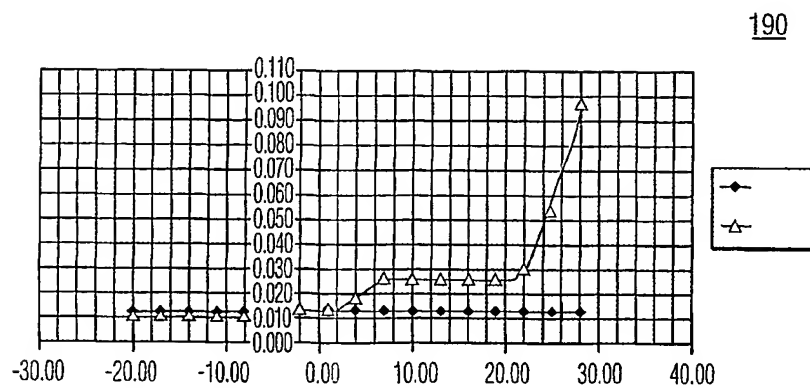


FIG. 7B

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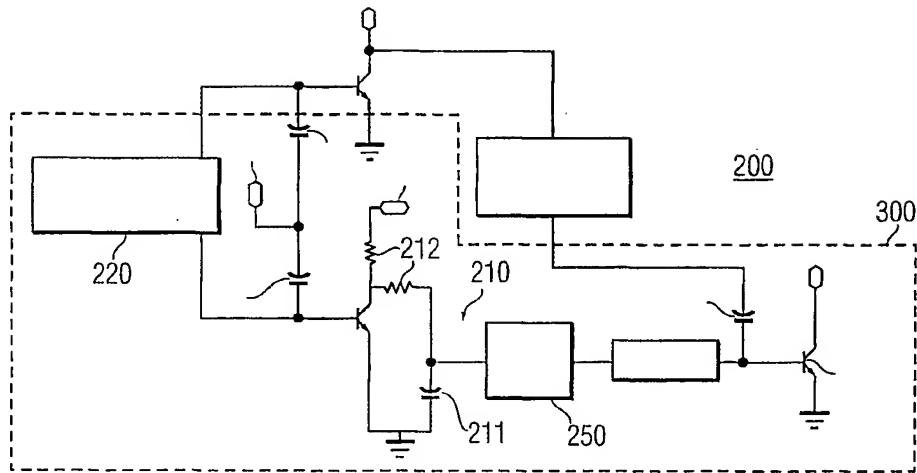


FIG. 8

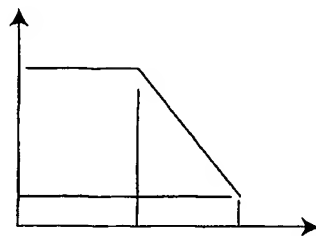


FIG. 9

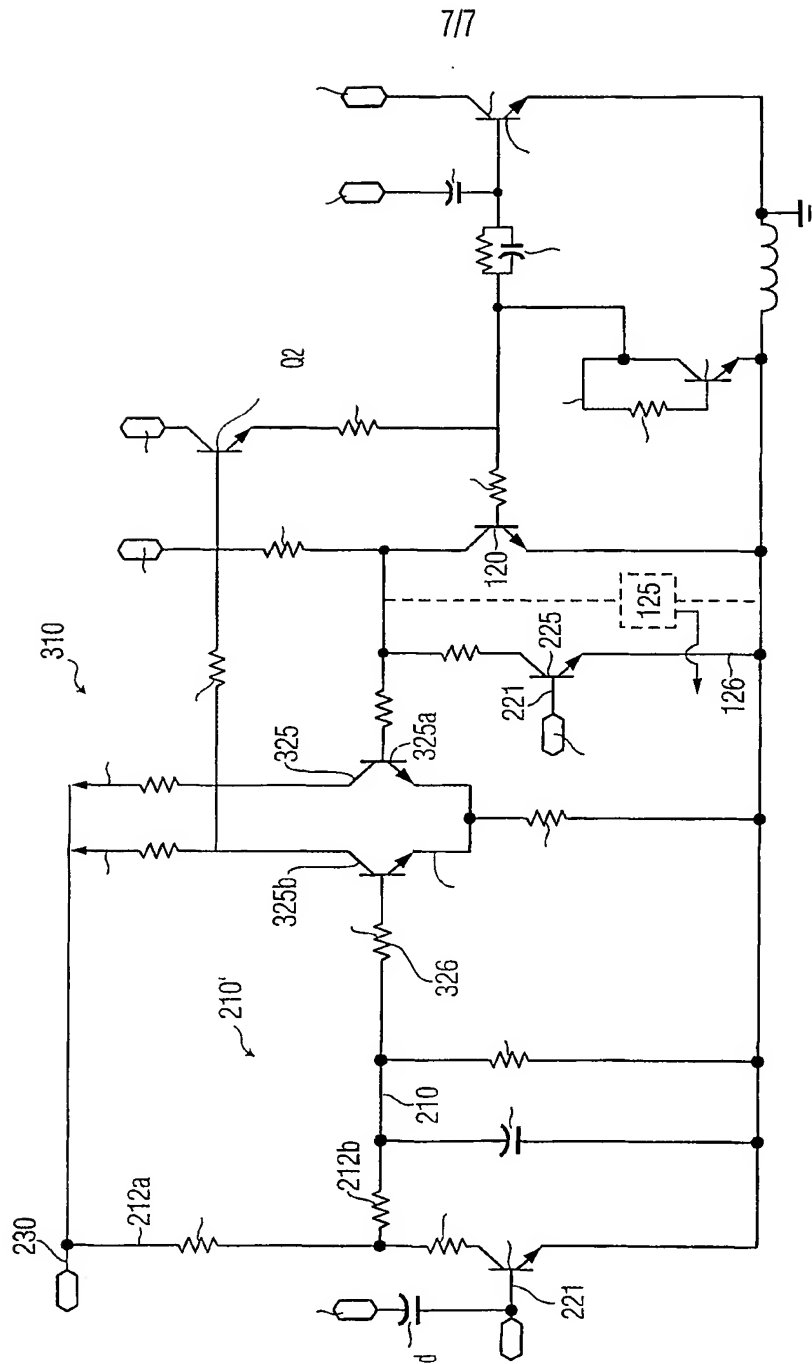


FIG. 10

INTERNATIONAL SEARCH REPORT

International Application No.

PCT/IB 03/05518

A. CLASSIFICATION OF SUBJECT MATTER
 IPC 7 H03F1/02 H03F1/30

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/036519 A1 (TSIVIDIS YANNIS P ET AL) 28 March 2002 (2002-03-28) the whole document	1,2,3,4, 7,8,9, 11,12
X	US 5 532 646 A (AIHARA YUKICHI) 2 July 1996 (1996-07-02) column 4, line 26 - line 34; claim 20; figure 7	1,5,7, 11,13
X	US 5 757 237 A (STAUDINGER JOSEPH ET AL) 26 May 1998 (1998-05-26) abstract; figure 2	1,5,7, 11,13
X	WO 02/065652 A (SIEMENS AG ; ZOBEK AUGUST (DE)) 22 August 2002 (2002-08-22) page 3 - page 4; figure 1	1,7,11
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☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

20 February 2004

Date of mailing of the international search report

01/03/2004

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INTERNATIONAL SEARCH REPORT

International application No
PCT/IB 03/05518

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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P,A	US 2003/016083 A1 (HUG JOHN JOSEPH ET AL) 23 January 2003 (2003-01-23) cited in the application -----	

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